## 2.3 A 32-Site 4-Channel Cochlear Electrode Array

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Cochlear prostheses have evolved significantly over the past twenty years. Over 90,000 such devices have been implanted to date, restoring functional hearing to many profoundly-deaf and severely hearing-impaired patients. A cochlear implant bypasses the failed hair cells of the inner ear to electrically stimulate the auditory nerve using 16-22 wire electrodes. Although such implants have been remarkably effective, there remain significant variations in speech perception among patients as well as difficulties in understanding tonal languages and appreciating music. A potential solution to these problems is to develop electrode arrays having significantly increased numbers of stimulating sites so that the arrays can more easily adapt to differing patterns of nerve survival and make use of multi-polar current shaping to increase pitch perception [1]. However, increasing the number of wire electrodes is precluded by the size of the cochlea, which tapers from a diameter of about 1mm to about 200μm over its length. Integrated array position sensors to help optimize array placement and minimize insertion damage [2] are also needed. This paper presents a thin-film cochlear electrode array (Fig. 2.3.1) that achieves high site density and incorporates on-board circuitry for stimulus generation and position sensing. The array is designed for use in animal (guinea pig) studies but offers the same features and site densities needed for a 128-site 16-channel human array.

The array uses a boron etch-stop to form a 2.5μm-thick silicon substrate [2] under stress-compensated silicon dioxide and silicon nitride dielectrics. A parylene overcoat can be defined at wafer level prior to the ethylene-diamine-pyrocatechol substrate release etch that separates the array from the wafer. The 8mm-long substrate tapers from a width of 500μm to 200μm and supports thirty-two 180μm-diameter iridium-oxide stimulating sites on 250μm centers. A 14μm-thick boron-diffused silicon area forms the base of the array, which remains outside the cochlea to support circuitry for current generation, site selection, and position sensing (Fig. 2.3.1). While single-level metal is sufficient to connect the circuitry to 32 sites, stress-controlled multilevel metal and on-chip monolithic circuitry will be needed for 128-site arrays for human use.

The 11-mask passive array process is compatible with on-chip circuitry [3]; however, to meet the area restrictions in small animals, hybrid circuitry has been used here to take advantage of smaller industrial feature sizes. Realized in 0.5μm AMI CMOS, the 2.4mm × 2.4mm circuit chip (Fig. 2.3.2) is flip-chip bonded to the cochlear array via 45 gold lead tabs formed using the array process (Fig. 2.3.3). An 8-lead polymeric cable connects the array to a hermetically-sealed electronics package [4] containing a microcontroller [5] along with a wireless interface for power and bidirectional data transfer.

The array communicates with the microcontroller using a 5-wire/SPI protocol. Sixteen-bit command words (Fig. 2.3.4) are serially clocked in on the data line (DIN), latched, and validated in an error detection block (Fig. 2.3.5). The array functions in one of two modes. The first configures the array for current stimulation, while the second is used to implement functions such as position measurement, system tests, and neural recording. In stimulation mode, current is output on four parallel channels, each of which is routed to one of eight sites. Level shifters translate the 0-3V signaling used on the input lines into the ±2.5V levels used by the site drive circuitry. The input data is used to control a site selection matrix as well as a DAC that generates the output current level for the addressed channel. A single 8b DAC is shared over four stimulus channels using sample-and-hold (S/H) circuitry to retain the current level for each channel during applied pulses. Each S/H output is buffered and applied to an analog current driver as shown in Fig. 2.3.6. The S/H voltage is converted to a drive current (I) and mirrored to the output stage (5I) as a biphasic stimulus current ranging from 0 to ±500μA (Fig. 2.3.7). The monopolar and bipolar auditory thresholds, the levels of current necessary to elicit an auditory percept, in guinea pig are 50μA and 300μA, respectively [1]. The biphasic current match is typically better than 1 percent, ensuring accurate charge balancing. The output voltage compliance range of ±2V is sufficient to support biphasic stimulation at ±500μA and 40nC. For situations requiring output currents of more than 500μA, multiple sites can be driven in parallel with reduced spatial resolution. Minimum pulse widths are 4μs with a maximum per-channel power dissipation of 2.5mW. An output impedance greater than 50MΩ is seen at the cascode current mirror output stage. Although the shared-DAC approach implemented here is vulnerable to stimulus droop due to S/H node leakage, it saves about 10% in die area as compared with a per-channel DAC design, and the output stimulus currents are sufficiently stable for use in-vivo. On-chip current calibration, site-impedance monitoring, and neural recording can be performed using the DTO line. Neural recording provides an objective means of monitoring an individual's physiological response to electrical stimulation and can assist in patient fitting - a feature especially important for infants and children who cannot readily convey threshold and maximum comfort current levels.

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*References:*
[1] P. T. Bhatti, B. Y. Arcand, J. Wang, N. V. Butala, C. R. Friedrich, and K. D. Wise, “A High-Density Electrode Array for a Cochlear Prosthesis,” *IEEE Int. Conf. on Solid-State Sensors and Actuators (Transducers’03),* pp. 1750-1753, June, 2003.
[2] J. Wang, M. Gulari, and K. D. Wise, “An Integrated Position-Sensing System for a MEMS-Based Cochlear Implant,” *Tech. Dig. of IEDM,* pp. 129-132, Dec., 2005.
[3] K. D. Wise, D. J. Anderson, J. F. Hetke, D. R. Kipke, and K. Najafi, “Wireless Implantable Microsystems: High-Density Electronic Interfaces to the Nervous Systems,” *Proc. IEEE*, vol. 92, no. 1, pp. 76-97, Jan., 2004.
[4] T. J. Harpster, S. Nikles, N. Dokmeci, and K. Najafi, “Long-Term Hermeticity and Biological Performance of Anodically-Bonded Glass-Silicon Implantable Packages,” *IEEE Trans. on Device and Materials Reliability*, vol. 5, no. 3, pp. 458-466, Sept., 2005.
[5] E. Marsman, R. Senger, M. McCorquodale, M. Guthaus, R. Ravindran, G. Dasika, S. Mahlke, and R. Brown, “A 16-bit, Low-Power Microcontroller with Monolithic MEMS-LC Clocking,” *IEEE Int. Symposium on Circuits and Systems*, pp. 624-627, May, 2005.

 

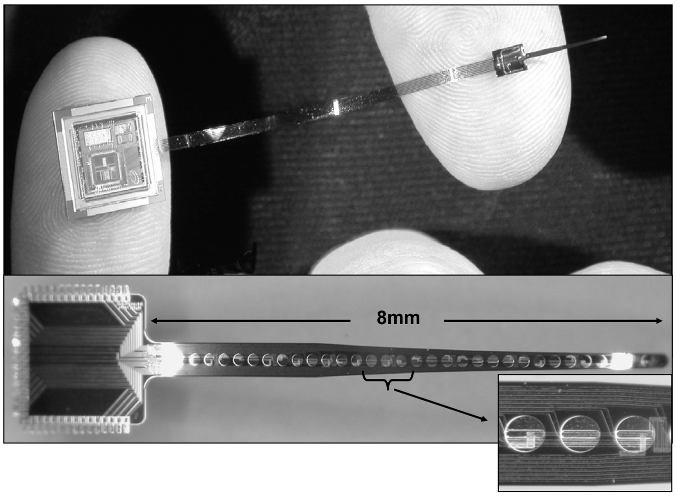


Figure 2.3.1: The 32-site 4-channel cochlear microsystem.

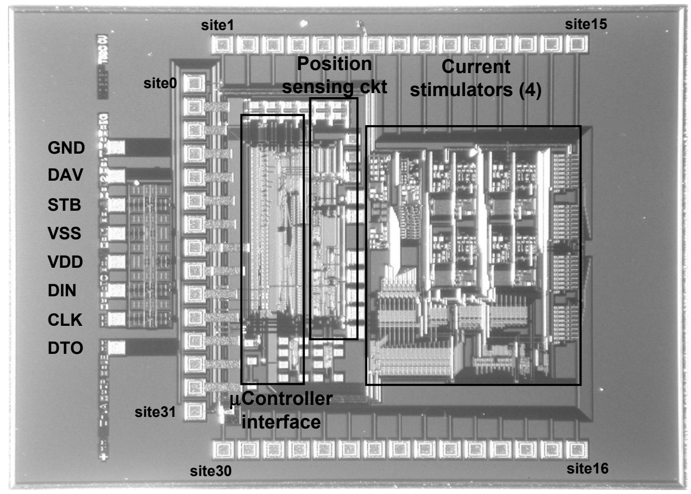


Figure 2.3.2: The circuit chip implementing the cochlear array electronics.

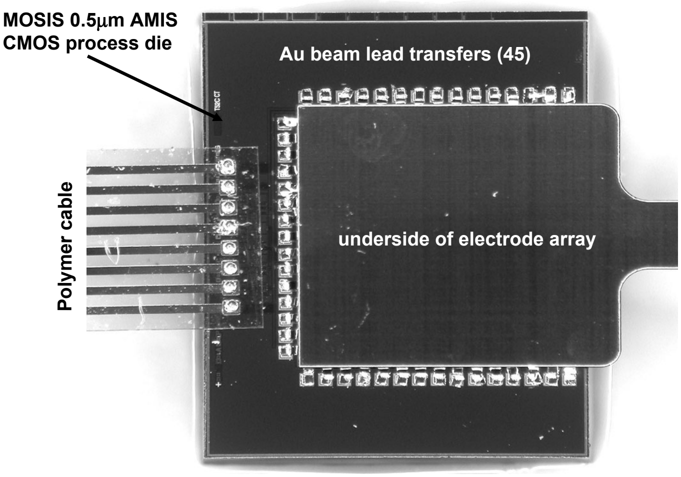


Figure 2.3.3: Hybrid interconnects between the microcontroller, the cochlear ASIC, and the electrode array.

| Signal | Input/Output/Power | Voltage Level |
|---|---|---|
| CLK | Input | 3V |
| DIN | Input | 3V |
| STB | Input | 3V |
| DAV | Output | -2.5 to 2.5V |
| DTO | Output | -2.5 to 2.5V |
| VDD | Power | 2.5V |
| VSS | Power | -2.5V |
| GND | Power | 0V |

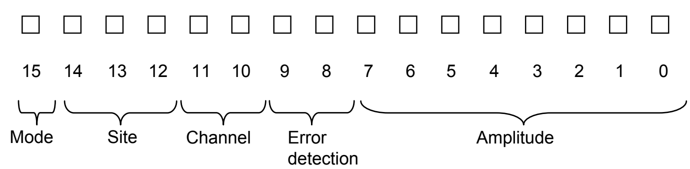


Figure 2.3.4: Designations for the eight cable leads and the input data word structure for the cochlear array.

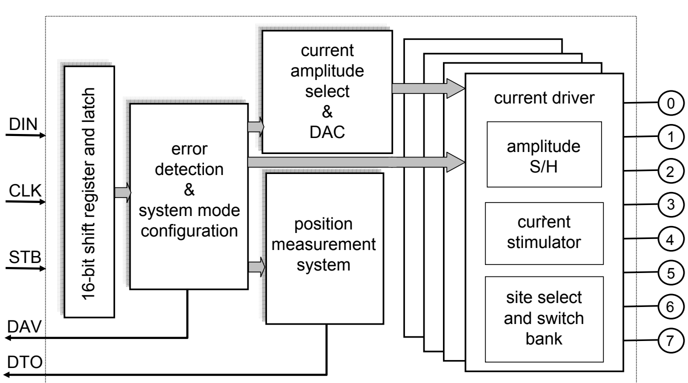


Figure 2.3.5: Block diagram of the cochlear array circuitry.

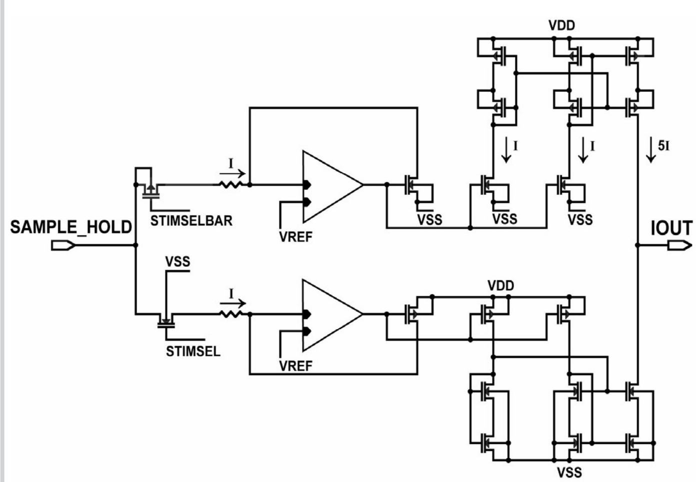


Figure 2.3.6: Schematic diagram of a stimulus output current driver.

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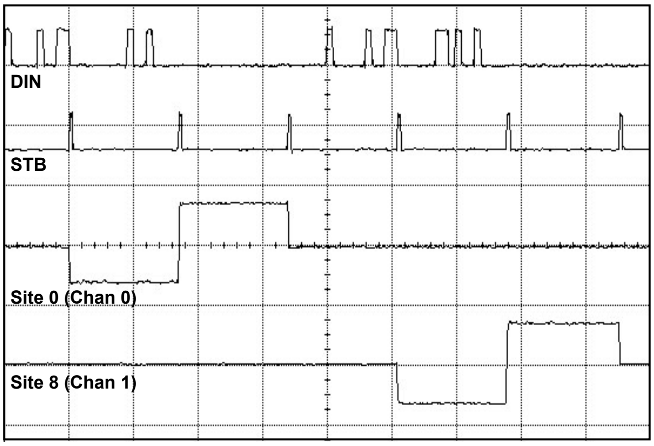


**Figure 2.3.7: Charge-balanced cathodic-first 140µA cochlear stimulation pulses on two parallel output channels (100µs/div, DIN and STB at 5V/div).**